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INTERFACE-STATE MEASUREMENTS OF GaAs SCHOTTKY BARRIERS USING ADMITTANCE TECHNIQUES: RELATIONSHIP TO BARRIER HEIGHT INSTABILITY

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With these assumptions in mind the following results were obtained. For the Au/Pt/Ti/GaAs diodes average interface-state densities in the low 10^{12} cm^{-2} eV^{1} were measured. These interface-state densities, like the barrier height, were not found to vary after aging under reverse bias conditions. In contrast, the Au/W/GaAs diodes had average interface-state densities in the mid to upper 10^{12} cm^{-2} eV^{1} range, which increased after reverse bias aging to the low to middle 10^{13} cm^{-2} eV^{1} range. This increase in interface-states points to at least a partial role of interface-states in the Fermi-level pinning of these aged Au/W/GaAs diodes.

It is not clear, however, what is causing the pinning in the Au/Pt/Ti/GaAs and the unaged Au/W/GaAs diodes. The concentration of states measured is probably not enough to pin the Fermi-level. Further study needs to be done in examining the role of fixed charge and deep levels in the pinning of the Fermi-level of these samples.

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INTERFACE-STATE MEASUREMENTS OF GaAs SCHOTTKY BARRIERS USING ADMITTANCE TECHNIQUES: RELATIONSHIP TO BARRIER HEIGHT INSTABILITY

Schottky diodes are employed extensively in GaAs microcircuits, being an intrinsic part of a MESFET structure. Understanding the mechanisms associated with degradations of the Schottky diode characteristics is a necessary condition for improving the reliability of GaAs microcircuits, which are being considered for inclusion in future systems.

This effort investigated the role of interface states in the degradation of GaAs Schottky barriers. Two methods of measuring the admittance of the Schottky barriers were investigated on two types of Schottky barriers. Barrier height drift was found to correlate with increases in the density of interface states as measured by admittance techniques.

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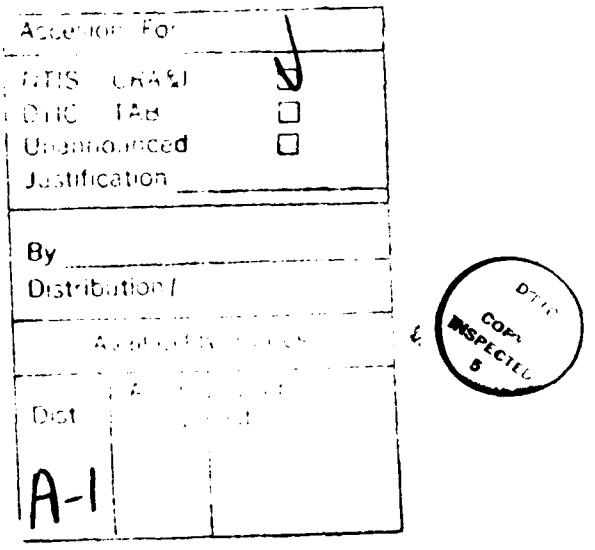

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by
Keith A. Christianson

ABSTRACT

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Two variations of the admittance technique were tried. The first variation, which looked for conductance variations as a function of frequency, was not successful, presumably due to the relatively large values of conductance already present in these structures making small variations impossible to see. The second variation looked at forward bias capacitance using a specially modified bridge circuit which enabled the large conductance signal to be nulled out. In order to obtain the interface-state densities from the forward bias capacitance data several assumptions had to be made so that existing theory could be applied. The first of these was that the responsible species are donor interface-states which reside in the upper half of the

bandgap. This selection allows for an increase in predominantly empty states to decrease the barrier height. These donor states were then assumed to have a constant capture cross-section, regardless of their aging or recovery history. Also, an estimate of the extent and composition of the interfacial layer had to be made for each group of samples.

With these assumptions in mind the following results were obtained. For the Au/Pt/Ti/GaAs diodes average interface-state densities in the low 10^{12} cm^{-2} eV^{-1} were measured. These interface-state densities, like the barrier height, were not found to vary after aging under reverse bias conditions. In contrast, the Au/W/GaAs diodes had average interface-state densities in the mid to upper 10^{12} cm^{-2} eV^{-1} range, which increased after reverse bias aging to the low to middle 10^{13} cm^{-2} eV^{-1} range. This increase in interface-states points to at least a partial role of interface-states in the Fermi-level pinning of these aged Au/W/GaAs diodes.

It is not clear, however, what is causing the pinning in the Au/Pt/Ti/GaAs and the unaged Au/W/GaAs diodes. The concentration of states measured is probably not enough to pin the Fermi-level. Further study needs to be done in examining the role of fixed charge and deep levels in the pinning of the Fermi-level of these samples.

I. INTRODUCTION

Metal/semiconductor contacts are a fundamental part of all discrete semiconductor devices and integrated circuits. Two main types can be distinguished: the ohmic (low resistance) and the Schottky (rectifying) type contacts. Despite the widespread usage of these contacts some fundamental properties are still not well understood, particularly those involving Schottky contacts on compound semiconductors.

For example, there is the question of barrier height. It is not understood why the barrier height of a metal on GaAs is relatively insensitive to the work function of the metal. A wide variety of metals give a barrier height of about 0.75 eV above the valance band for n-type GaAs, and about 0.5 eV above the valance band edge for p-type GaAs.[1] A number of theories have been proposed to explain the pinning of the Fermi level, including the unified defect model by Spicer[2,3] and the effective work function model by Woodall.[4] There is no general agreement at this point on the responsible mechanism.

In addition to not understanding what causes the barrier height to be fixed at relatively constant level, a new series of experiments have changed the barrier height, temporarily, after photochemical and/or chemical treatments.[5,6] Also, a recent series of measurements have shown that the barrier height of Schottky diodes on GaAs may change under biasing conditions. The effect has been most pronounced for Ag/GaAs and W/GaAs diodes, but has also been observed in Au/GaAs and Ti/GaAs diodes.[7,8] The aging has been found to occur under reverse bias conditions with a logarithmic dependence on time. Recovery of the barrier height was found to occur within a few days of removal of the bias, or in an accelerated manner under forward bias. The slow time constant associated with this process suggests that creation/destruction of interface-states/deep levels is occurring.

The understanding of the mechanism(s) behind this barrier height shift will require the careful characterization of the trapping states present in those devices which show this instability. In general these characterization techniques rely on analysis in either the time or frequency domai: The time domain techniques include both capacitance[9] and current[10] deep level transient spectroscopy (DLTS). These techniques are widely used for the analysis of bulk trapping levels, but the interpretation of the results becomes much more difficult for interface-states. The characterization of devices which show these aging effects with DLTS techniques has been addressed in a separate proposal funded by AFOSR/UES.[11]

Frequency domain techniques are also used to analyze the interface-states present in Schottky barriers. The measurement procedures used are a variation of the admittance techniques.[12] There seems to be agreement that it is not appropriate to use the MOS model to determine the interface-state density and energy configuration from the admittance measurements. However, the exact model to be used in the analysis is currently the source of controversy. This model should incorporate the conductance of the diode when the sample is in forward bias. The model should also accomodate the fact that at least some of the interface-states under certain conditions are more communicative with the metal than with the semiconductor, i.e. such states follow the metal Fermi level.

One recent model has been suggested by Ho et al.[13] with continuing work by Wu and Yang.[14] In this model the diode capacitance is taken to be due to the modulation of the effective Schottky barrier height by the interface charge. In many respects this model is beginning to resemble that suggested by Werner et al.,[15] particularily with respect to the way the capacitance is modeled. Also, a very recent theoretical paper by Nannini and Bagnoli[16] has

suggested a way to model the capacitance of conducting MIS structures with one distribution of states tied to the Fermi level of the metal and a second distribution of states tied to the Fermi level of the semiconductor. It should be possible to incorporate the work of Nannini and Bagnoli[16] into the model of Wu and Yang[14] in order to allow for random distribution of states at the interface and within the oxide itself, if appropriate.

II. OBJECTIVES OF THE RESEARCH EFFORT

The major objective of this research effort has been to see if there is a connection between the interface-state configuration of GaAs Schottky barriers and their barrier height aging characteristics. This was to be accomplished by using two variations of the admittance technique to evaluate the interface-state characteristics. The first variation to be used was the technique of Werner,[15] which involves measuring the forward-bias conductance at a number of frequencies and forward biases. The second variation used the technique of Ho et al.[13] and more recently developed by Wu and Yang.[14] Using this variation forward-bias capacitance measurements were made at a single frequency as a function of forward bias, and also at multiple frequencies at the forward voltage response peak. The models associated with these two admittance variations were to be used to evaluate interface-state concentration and energy position of both aged and non-aged diodes. Both samples susceptible to aging as well as those not were to be examined.

In addition, results from the DLTS study funded by AFOSR/UES[11] will be compared to interface-state measurements made on the same samples by admittance techniques. In this manner it will be possible to compare the two major techniques for interface-state measurements (DLTS and admittance),

and to evaluate the accuracy of the models developed for them thus far. Results from both the DLTS and admittance measurements will be used to aid the modeling of the mechanism responsible for the observed barrier height shifts. This comparison will be contained in the final report for the AFOSR/UES grant.

III. EXPERIMENTAL PROCEDURE

A. Samples

The same two groups of samples previously evaluated in the barrier height aging study were used in this study.[8,17] The first group were GaAs power MESFETs, designed for two watts output at 7.5 GHz. They have 24 gate fingers, each 200 μm wide by 1 μm length, for a total gate width of 4.8 mm. The metalization system for the gate was Au/W/GaAs. The second group of samples were also GaAs power MESFETs, however this group of samples was designed for two watts output at 4 GHz. Their structure has six gate fingers, each 1 μm length, with a total gate width of 1.7 mm. The metalization system for these is Au/Pt/Ti/GaAs. Further details about these samples may be found in references (8) and (17).

The use of MESFETs instead of simple Schottky barriers has once again complicated the investigation. With the MESFET the gate-source, gate-drain, and gate-source and drain connected together can all be examined. For this investigation the gate-source diode of the Au/W/GaAs devices were examined, while the gate-drain diode of the Au/Pt/Ti/GaAs devices were examined. These connections were chosen since the devices were previously seen to exhibit the greatest amount of aging when connected in this manner.[8]

B. Evaluation of barrier height aging

Samples for this project were evaluated for their I-V properties in an automated manner using an HP 4062A semiconductor parameter analyzer. The extent of barrier height aging of the devices was then determined from the I-V properties by substitution into the thermionic emission equation:

$$I = SA^{**}T^2\left(\exp\frac{-\phi_{b0}}{V_T}\right)\left(\exp\frac{V-IR}{nV_T} - 1\right) \qquad (1)$$

where I is the current, S is the area, A** is the modified Richardson constant (taken to be 8.1), T is the temperature, ϕ_{b0} is the zero bias barrier height, V_T is the thermal voltage, V is the sample voltage, R is the sum of contact and bulk resistances and n is the ideality factor. A plot of log I vs $V_{forward}$ should be a straight line, with the slope yielding the ideality factor n:

$$n = \frac{1}{kT}\frac{\delta V}{\delta \ln I} \qquad (2)$$

This slope was obtained by a least squares fit over the linear portion of the forward bias curve. An estimated current was then obtained at V = 0.30 V followed by extrapolation to zero bias to get ϕ_{b0}.

As can be seen from equation (1) there is a strong temperature dependence in the thermionic process. To forestall problems, the sample temperature was monitored and recorded at each measurement step, and the updated value used in the calculation. Also, since the case temperature is not an accurate measure of the junction temperature, the ideality factor was watched for drifting after bias aging as per Miret et al.[7] In all cases the estimated temperature rise was less than 5 K.

C. Measurement of interface-state parameters

1. Forward bias conductivity

The forward bias conductance as a function of frequency was measured with an HP 4275A LCR meter over the frequency range of 10 kHz to 4 MHz. Bias to the sample was provided by an HP 6033A system power supply connected through the external bias connection available on the back of the LCR meter. The forward bias conductance was also measured over the frequency range of 100 Hz to 100 kHz using the lock-in amplifier based bridge described in the next section.

2. Forward bias capacitance

The HP LCR bridge previously mentioned was not suitable for the measurement of the forward bias capacitance of the samples because the capacitance is of relatively small magnitude compared to the conductance. If the phase accuracy of this bridge is less than perfect, the capacitance signal will be overwhelmed by the conductance signal and the bridge will give erroneous results. To overcome this problem the measurement system of Wu et al.,[18] which is based on the work of Evans et al.[19] and the work of D.W. Greve,[20] has been implemented in a modified version.

Figure 1 shows the apparatus which was used to measure the forward bias capacitance, and can also be used to measure the forward bias conductance. The operation of this apparatus is similar to the measurement system used to measure MOS capacitance with the exception that the inverting input of the lock-in amplifier is also used in the following manner. First, with the phase of the lock-in set to measure the capacitance signal the -B input is examined. The phase vernier of the lock-in is then set so that no output is obtained. Next, the phase range switch of the lock-in is changed 90° and the

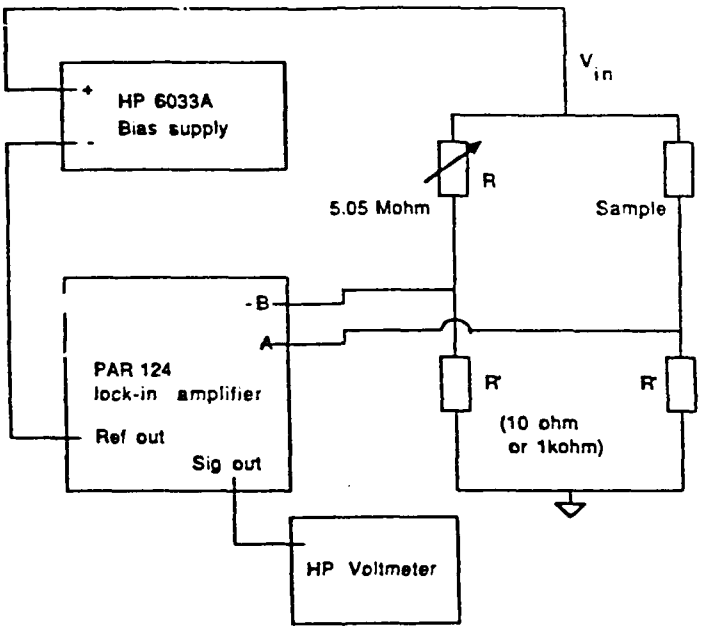

Fig. 1. Schematic representation of the experimental apparatus used to make forward bias capacitance measurements.

input A-B is examined. The magnitude of the variable resistor R is then changed until zero output is obtained. At this point the phase range is changed by 90° and the capacitance component of the sample is examined. Because the conductance part of the sample admittance has been nulled out externally, relatively small amounts of phase error do not give erroneous capacitance values.

If the magnitude of the impedance of the R' resistors is kept small compared to the magnitude of the sample impedance the voltage across the sampling resistor is given by voltage division as:

$$V_a = 2 \pi f C R' V_{in} \qquad (3)$$

The selection of 10 or 1000 Ω resistors in the circuit allows for this criteria to be met while at the same time allows for an appropriate sensitivity to be selected. In practice the 10 Ω resistor was used for conductance measurements, while the 1 kΩ resistor was used for the smaller magnitude of the capacitance signal. In all cases the ac measurement signal from the lock-in was 10 mV (rms). The results of these measurements were curve fitted to the expressions of Wu and Yang,[14] as will be explained in the experimental results section.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Au/Pt/Ti/GaAs Schottky barriers

1. Barrier height aging results

With the aging values selected for this experiment ($V_{g\text{-source, drain}} = -10$ V) no aging was observed in the barrier height or ideality factor of the Au/Pt/Ti/GaAs samples tested. Figure 2 shows this for a 12 hour age for sample

#7. Additionally, Figure 3 shows the forward I-V characteristics of this sample, which are needed as an input in the forward-bias capacitance interface-state calculations. For forward biases greater than 0.2 V it is seen from the linear nature of the curve that thermionic emission is dominant. Also, the ideality factor is small at approximately 1.1. If this ideality factor is attributed to a combination of the interfacial-layer and the series resistance (see Appendix) then the contribution from these to diode performance is also small.

2. Forward bias conductance results

Over the frequency range covered by the LCR meter and the lock-in amplifier based bridge no variation in the conductivity as a function of frequency could be detected. Thus, it was not possible to use Werner's technique[15] to evaluate interface-state densities, since this depends on being able to see such a variation. The observed conductance values (on the order of 10^{-6} to 10^{-3} S) were more than 3 orders of magnitude greater than that of Werner's samples, which indicates the variations may not have been observable due to the large value of conductance present. The large values of conductance are attributable to the fact that the devices tested are power microwave devices, which are specifically designed to have a small value of contact and channel resistance.

Because the model used for forward bias capacitance also requires values of the small signal ac conductance as a function of forward bias these are given in Figure 4 for a typical Au/Pt/Ti/GaAs device.

3. Forward bias capacitance results

Forward bias capacitance measurements were taken in order to allow for interface-state evaluation using the method of Wu and Yang.[10] The

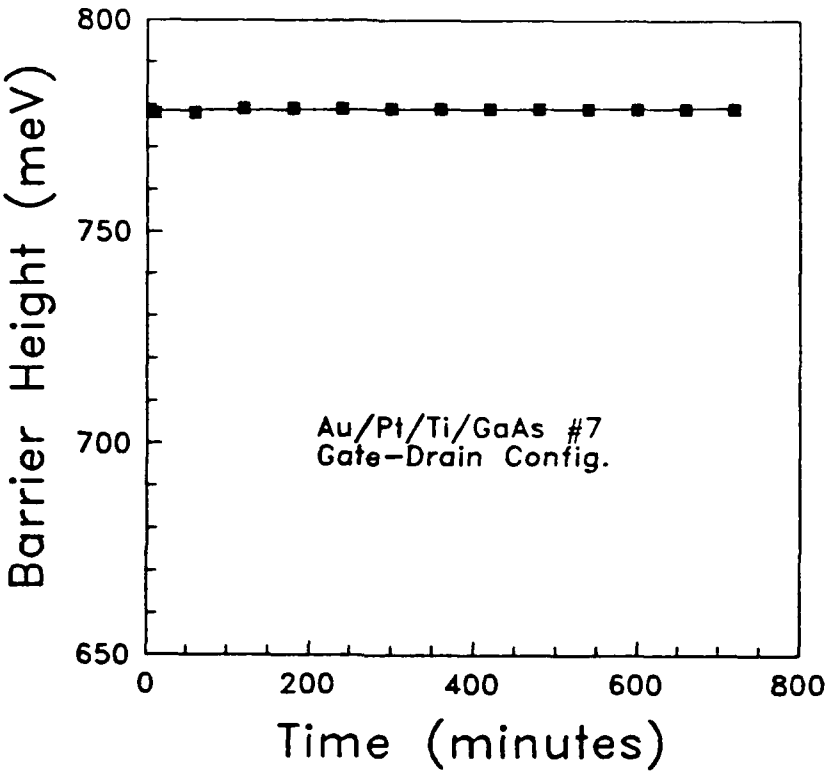

Fig. 2a. Barrier height versus aging time for a typical Au/Pt/Ti/GaAs Schottky barrier. Aging voltage was -10 V. Line is best linear fit to the data.

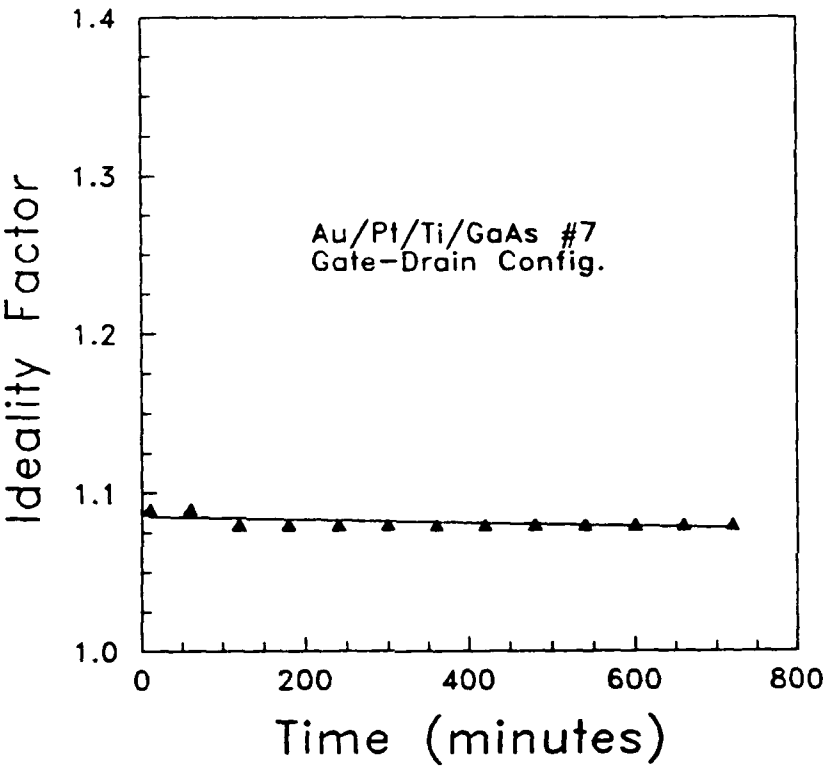

Fig. 2b. Ideality factor versus aging time for a typical Au/Pt/Ti/GaAs Schottky barrier. Aging voltage was -10 V. Line is best linear fit to the data.

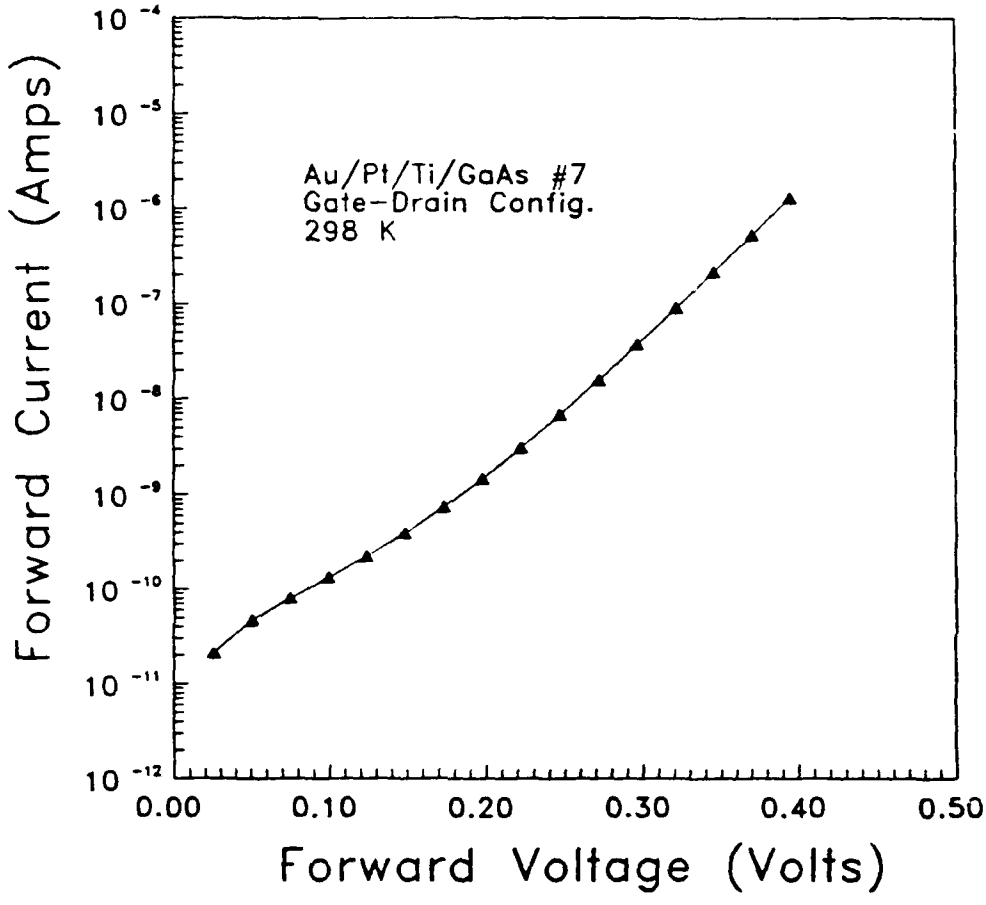

Fig. 3. Forward I-V characteristics of a typical Au/Pt/Ti/GaAs Schottky barrier. Line is eye aid only. Slope was determined as described in reference (17).

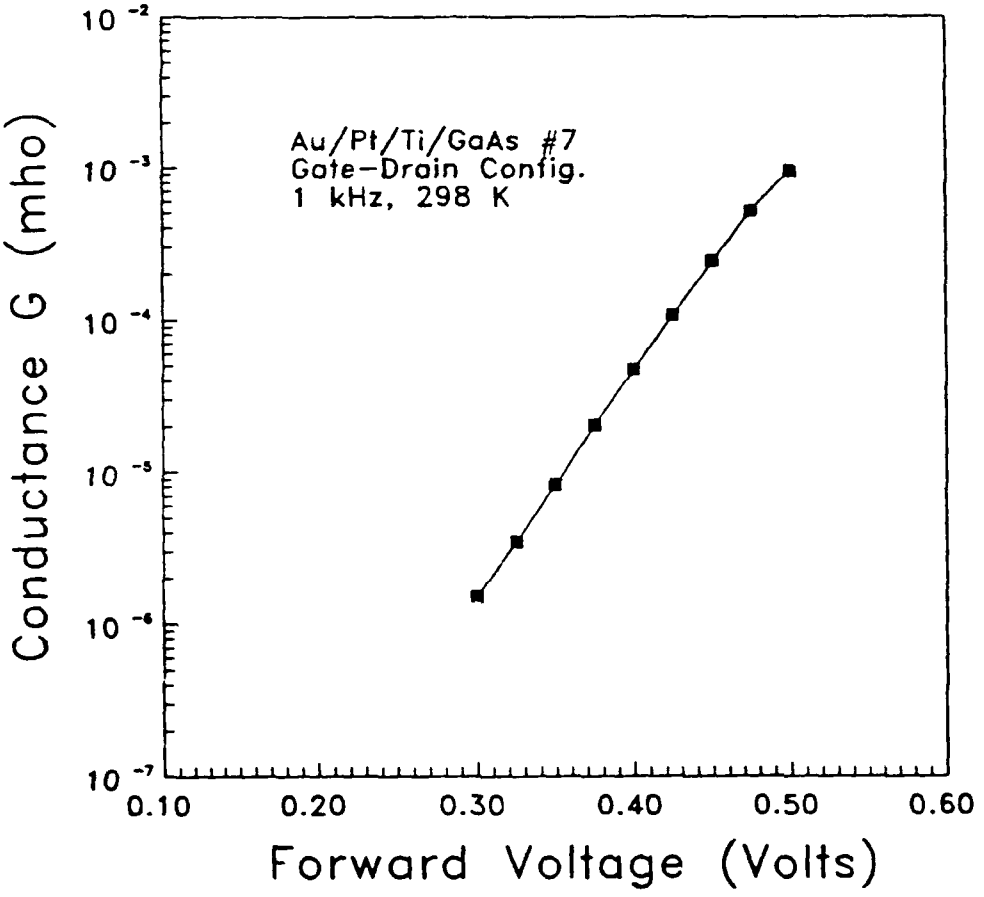

Fig. 4. Conductance at 1 kHz versus forward voltage for a typical Au/Pt/Ti/GaAs Schottky barrier. Line is eye aid only.

primary goal was to curve fit to expression 21 of the method as was developed in his paper. This expression has also been derived more completely in the Appendix of this report. The pertinent expression is:

$$\omega C = \frac{q^2 I}{kT\left(1 + qR_s J / kT\right)} \frac{N_S\left(E_f^s\right)}{C_i \Delta V} \times \frac{\omega(1-f)\, 4\sigma_n j / q}{\left(4\sigma_n J / q + 1/\tau_m\right)^2 + \omega^2} \tag{4}$$

In order to allow for comparison with the experimental data, it would be desirable to be able to locate any extrema of this expression. Taking the derivative of this expression with respect to the voltage is rather difficult, since any voltage dependence is implicit in the current terms. However, if we look at the expression as a function of angular frequency we see that it is of the form:

$$B \alpha \frac{\omega}{a^2 + \omega^2} \tag{5}$$

which has a maximum at $a = \omega$. Thus it is possible to define an expression involving the capture cross section, the dc current density, the time constant of the relaxation of the carriers into the metal, and the maximum of the capacitance response as a function of frequency.

At this point Wu and Yang[14] took a limiting low frequency case in order to solve for the capture cross section and the relaxation constant independently. The assumptions involved in this step are rather questionable, and in any event do not apply to the samples evaluated in this study. This is because the sample capacitance of the diodes looked at in this study are much smaller than that of Wu and Yangs (approximately 10 pF versus a few nF), and

thus no data could be taken at the portion of the frequency spectrum where these assumptions (might) apply.

Instead of Wu and Yang's procedure, an assumption as to the value of the capture cross section was made. It is believed that the interface-states present and being made by the aging process are responsible for making the barrier height decrease. This implies that these states have a positive charge associated with them, according to two different theories of the relationship between barrier height and charge at the interface.[21,22] Interface donor states located in the upper half of the bandgap will give such behavior, if we assume that the majority of them are empty and thus are in their positive charge state. As a part of the evaluation of interface-state densities from forward bias capacitance the occupation factor for these states is calculated, and it will be seen that it is less than 25%. Such donor states typically have a capture cross section of approximately 10^{-14} cm^{-2},[23] and this value will be used for calculations involving both the Au/Pt/Ti/GaAs and the Au/W/GaAs samples.

Note that the rest of this work thus assumes that the capture cross section does not change with aging. This may not be true, in fact for Si MOS transistors subjected to hot-carrier aging a very recent study has indicated that the cross section varies between aged and non-aged samples.[23] With the samples and instrumentation used in this study, however, it was not possible to distinguish between concentration variations and cross section variations. In order to allow for an evaluation of the experimental data it was thus assumed that the the concentration of the interface-states is the independent parameter.

The validity of this assumption is somewhat strengthened by the measurement of interface-state densities based upon I-V characteristics

(which at their present stage of theory development does not depend on capture cross section) of the few samples (unfortunately all Au/W/GaAs, however) whose reverse characteristics are not totally dominated by *thermionic-field emission.*[24] These samples show interface-state densities in the same range as those measured in this study.

In order to evaluate for the interface-state density it is also necessary to have a value of the interface layer specific capacitance, C_i. For these samples it is assumed that the interface is composed of GaO, which has an relative dielectric constant of 3.5.[25] Also needed is a value of δ, the interfacial layer thickness. For this grouping of samples it was assumed this value is 10 Å, which is typical of good technology at the time these samples were manufactured.[26] Evaluation for this capacitance, using equation 7 of the Wu and Yang's paper, gives a value of 3.1×10^{-6} F/cm^2 for these samples.

The assumption of these two parameters, along with the assumption of the non-changing capture cross section, are the major assumptions of this analysis. In the conclusions and recommendation section ways to test the validity of these assumptions will be suggested.

With these assumptions we are now ready to evaluate for interface-state density of the Au/Pt/Ti/GaAs samples using forward-bias capacitance. Measurements were made both before and after aging of the samples for a twelve hour period corresponding to the beginning and end of the aging cycle shown in Figure 2. Neither of the susceptance curves nor the conductance curve showed any variation after aging beyond that which could be attributed to experimental error, and thus for clarity only the not aged data set is shown for each sample. Figure 5 shows the susceptance of a typical sample, #7, as a

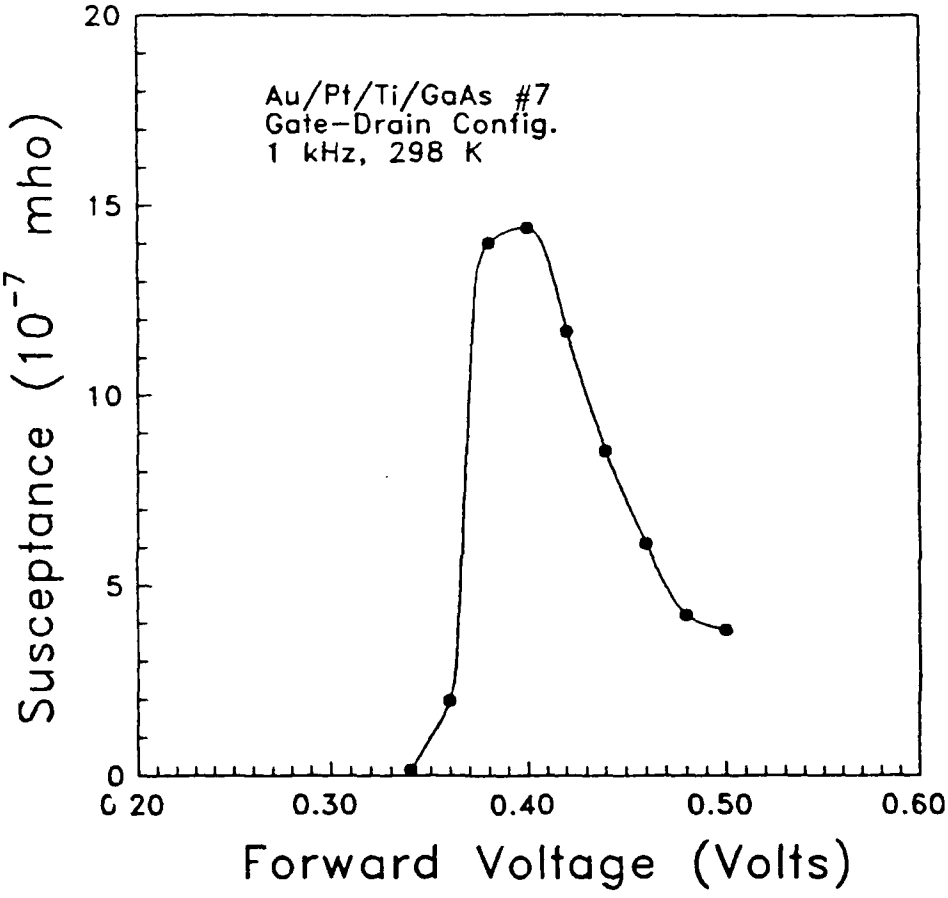

Fig. 5. Susceptance versus forward voltage for a typical Au/Pt/Ti/GaAs Schottky barrier. Line is eye aid only.

function of forward-bias. From this figure a peak at 0.40 V forward bias is observed with a value of 1.5 x 10^{-6} S. From the susceptance versus frequency curve, Figure 6, for the same sample taken at the forward bias for a maximum response (in this case 0.40 V) a peak is observed at a frequency of 10 kHz. From this frequency response peak a value of τ_m of 1.6 x 10^{-5} seconds was obtained using equation 27 of Wu and Yang. Then, from equation 14 of Wu and Yang, a value of 0.23 for the occupation factor was obtained.

Evaluation for the interface-state density also required the dc current density, J, and the ac current density, j, at the voltage of the maximum response. These were obtained from Figures 3 and 4 for the dc and ac values respectively, after dividing by the device area (in this case 1.712 x 10^{-5} cm^2). The value of the test voltage in all cases was 10 mV rms, which is referred to in this expression as ΔV. The series resistances were assumed to be negligible, and thus R_S was set equal to zero.

With the preceeding as inputs the model of Wu and Yang,[14] as further developed in the appendix, gives a value of $N_S(E_f^s)$ of 9 x 10^{11} cm^{-2} for the two samples tested. If we remember what this notation means it is the interface-state density evaluated at the position of the Fermi-level, and it possible to evaluate for an average interface-state density using the relationship:

$$N_S\left(E_f^s\right) = \int_{E_f^m}^{E_f^s} N_{SS}(E)\,dE = \overline{N}_{SS}\, q\, V_A \tag{6}$$

With this an average interface density N_{SS} is calculated to be 2 x 10^{12} cm^{-2} eV^{-1} for these samples. Evaluation of the energy dependence of the observed states within the bandgap was not deemed worthwhile at this point because it depended on graphical differentiation of the response curve of the susceptance as a function of forward bias (which is nearly a vertical line at

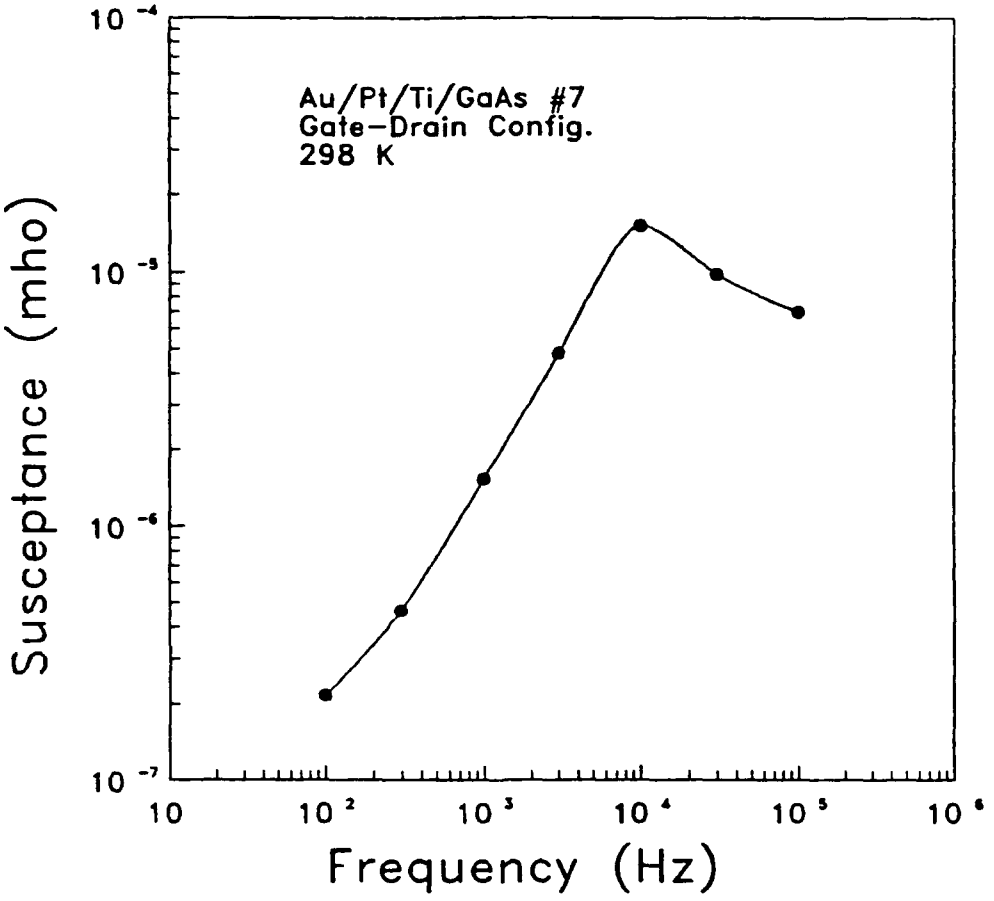

Fig. 6. Susceptance versus frequency for a typical Au/Pt/Ti/GaAs diode. Testing voltage was 0.40 V. Line is eye aid only.

the low voltage end of the response). An alternate technique is possible, which depends on the movement of this response curve as a function of temperature. A suitable, i.e. temperature stable, cryostat was not available to use this approach.

If this gate metalization (Au/Pt/Ti/GaAs) is viewed as typical of a reactive interface, then the following should be noted. First, there is relatively little oxide at the interface, as has been evidenced in the Auger spectrum,[8] the low value of the ideality factor, and the measurement of the Richardson constant to be near the theoretical value.[24] The concentration of interface-states measured is not enough to account for the Fermi-level pinning, however, which by most currently accepted theories[27,28] would require a density greater than measured, perhaps near 10^{13} cm^{-2} eV^{-1}. It might be possible to account for this variation by changing the assumed value of the capture cross section, but this value was already chosen to be rather large and it would be difficult to justify making it even larger without specific knowledge or reason to do so.

Given this information, what is pinning the Fermi-level of these samples, or equivalently causing the barrier height to be fixed? One possible explanation is fixed charge, where we are using the definition of fixed charge as that charge which does not respond to the application of an electric field. Presumably this fixed charge will not be measured in these capacitance measuring experiments, however, when the oxide thicknesses are so small it becomes very difficult to sort out the contribution of tunneling to these sorts of measurements. A recent experimental work[28] by Sobolewski and Helms has examined metal-silicon nitride-silicon Schottky diodes, and has concluded that the interface-state density is not large enough to account for the Fermi-level

pinning. By fabricating diodes of various interfacial layer thicknesses, the authors where able to show that fixed charge and band lineup at the interface were able to account for the Fermi-level pinning. It was not possible to duplicate their experiment here because the samples examined in this study were presumably fabricated with an equal oxide thickness.

The other possible mechanism for Fermi-level pinning in this case are interface-states with a very long time constant, i.e. slow states. Some recent results[29] in the MOS system have shown both fast and slow interface-states being made in the hot-carrier aging process. Presumably if slow interface-states are pinning the Fermi-level in these GaAs Schottkys they could be too slow to measure with the current experimental apparatus. Once again the difference between fixed charge, which could perhaps tunnel, and slow interface-states seems to be one of semantics.

B. Au/W/GaAs Schottky barriers

1. Barrier height aging results

Considerable aging in the barrier height and ideality factor were observed for the Au/W/GaAs samples after a twelve hour age at -10 V. The amount of aging observed (approximately 60 meV drop from an initial barrier height of 730 meV) was comparable to that observed in the previous investigation.[8,17] Typical results are shown in Figure 7 for sample #20. Also, since the dc forward bias characteristics are required as an input to the forward bias capacitance results, these are shown in Figure 8 for the same sample in the not aged and aged condition. The forward characteristics are well behaved over the forward bias regime tested in a manner consistent with thermionic emission. The not aged ideality factor for these Au/W/GaAs diodes

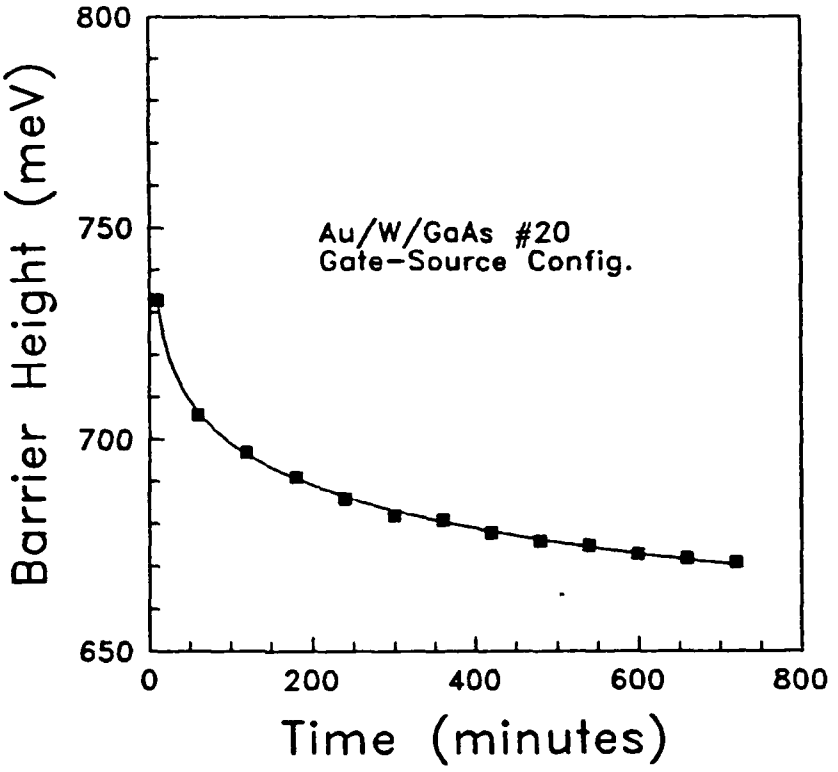

Fig. 7a. Barrier height versus aging time for a typical Au/W/GaAs Schottky barrier. Aging voltage was -10 V. Line is best logarithmic fit to the data.

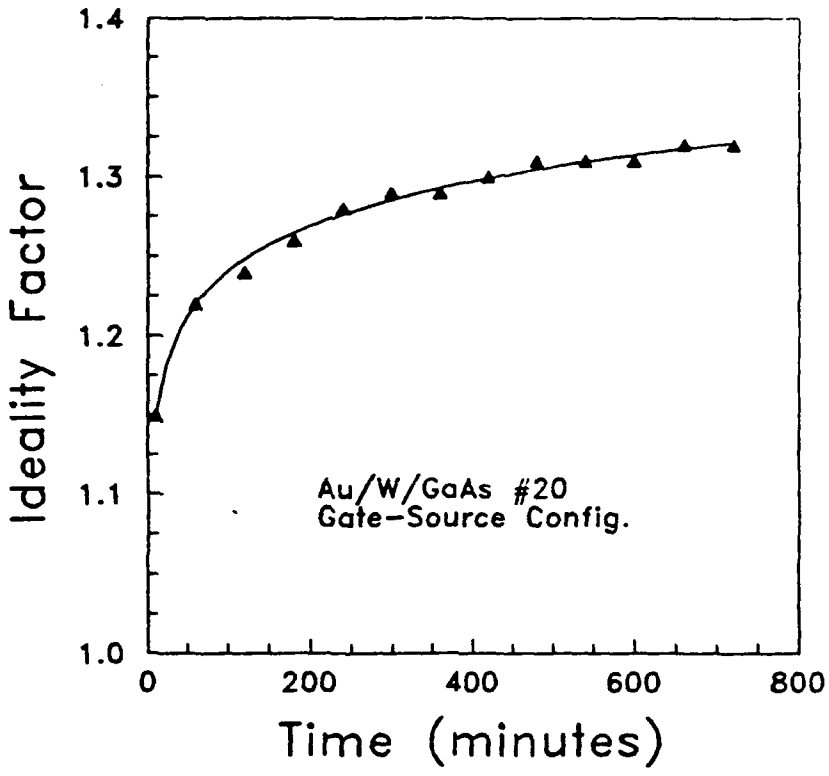

Fig. 7b. Ideality factor versus aging time for a typical Au/W/GaAs Schottky barrier. Aging voltage was -10V. Line is best logarithmic fit to the data.

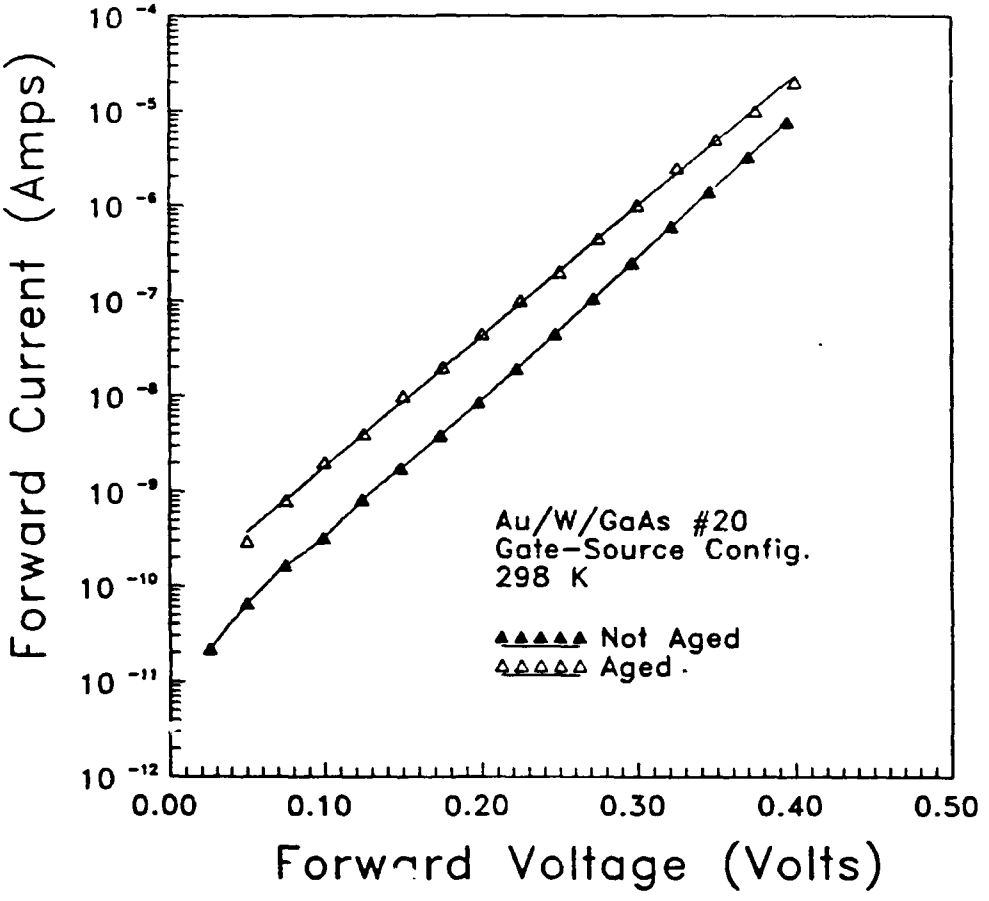

Fig. 8. Forward I-V characteristics for a typical Au/W/GaAs Schottky diode not aged and after aging at -10 V for 12 hours. Line is eye aid only. Slope was determined from these points as described in reference (17).

is larger than that for the Au/Pt/Ti/GaAs diodes (n = 1.2 versus 1.1). Once again if this ideality factor is associated with the interfacial layer and/or series resistance the slightly larger value indicates a greater role in device performance for this interfacial layer and/or series resistance. Most likely the interfacial layer is playing the greatest role here since Auger results[8,17] have shown a greater amount of oxide at the interface for these W-gated samples than for the Ti-gated samples, and also because the conductance values of the two sets of samples are roughly the same.

2. Forward bias conductance results

Once again it was not possible to resolve any variation in the ac conductance as a function of frequency, presumably because of the large value of conductance already present (on the order of 10^{-6} - 10^{-3} S). Because the interface-state calculations require a value of the ac conductance at the testing voltage, Figure 9 shows the ac conductance as a function of voltage for a typical Au/W/GaAs sample in the not aged condition and following a 12 hour age at -10 V. Notice the increase in current at all voltages for the aged case as would be expected for the observed decrease in barrier height.

3. Forward bias capacitance results

Since the details of extracting the interface-state density from the forward-bias capacitance results have been covered in a previous section, only those changes to the theory which are necessary to accurately extract values for this set of samples will be discussed here. All assumptions mentioned previously, including the use of a fixed capture cross-section, are still being applied if no mention is made here of them.

The largest change is in the value of interface specific capacitance, C_i. Because of the evidence for a more dominant interfacial layer (from the Auger

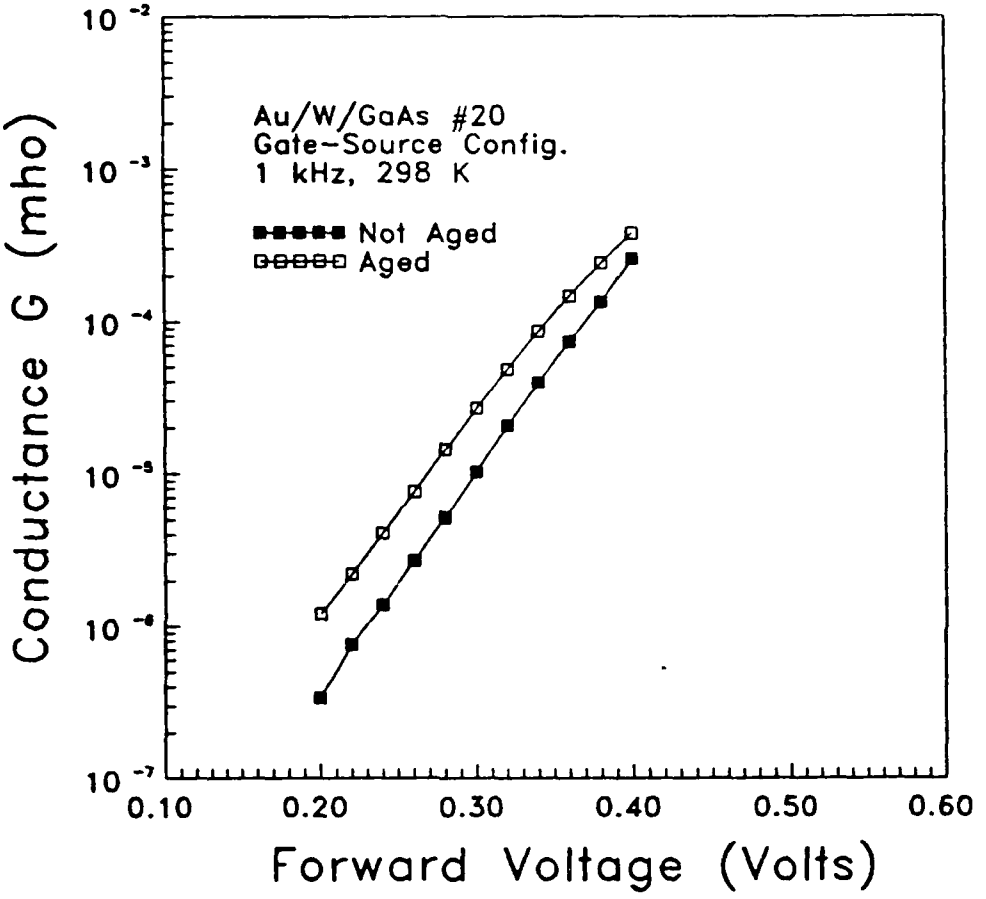

Fig. 9. Conductance as a function of forward voltage for a not aged Au/W/GaAs Schottky barrier and the same diode after twelve hours at -10 V. Conductance was measured at 1 kHz. Line is eye aid only.

results,[8,17] the ideality factor, and also the greater deviation of the experimentally measured Richardson constant from the theoretical value[24]) the thickness assigned to this layer is greater than that used for the Au/Pt/Ti/GaAs diodes. A value of 25 Å was selected. This value was chosen since it has been shown[25] that under poor preparation techniques that a limiting value of about 30 Å of oxide is present on the surface, and it is assumed that the surface preparation was slightly better than worst case.

The relative dielectric constant has also been evaluated separately from the I-V characteristics of a few of these diodes in a manner suggested by Harvath.[30] For those samples whose reverse characteristics are not totally dominated by thermionic-field (TF) emission a relative thickness (interfacial layer thickness divided by relative dielectric constant) was calculated. For the sample being shown here this value was 6.7 x 10^{-8} cm. If an oxide dielectric constant of 3.5 is assumed, the interfacial layer thickness may then be calculated to be 24 Å.[24]

The susceptance of the samples was once again measured in the aged as well as not aged condition. For these samples, however, quite a remarkable change was seen between the aged and not aged diodes in their susceptance as a function of forward bias. Figure 10 shows the susceptance as a function of forward bias of a typical Au/W/GaAs sample (#20) both before and after aging for 12 hours at V_{gs} = -10 V. After aging the peak height has increased slightly, and the voltage at which the peak occurs has shifted from 0.36 V to 0.30 V. In contrast, the susceptance peak as a function of frequency does not change with aging, but instead stays constant at 30 kHz as Figure 11 shows. Using the same method of evaluation as before the not aged average (N_{SS}) interface-state density has been calculated to be in the range of 5-10 x 10^{12} cm^{-2} eV^{-1}, which changes to 3-4 x 10^{13} cm^{-2} eV^{-1} after aging for 12 hours with V_{gs}=-10 V.

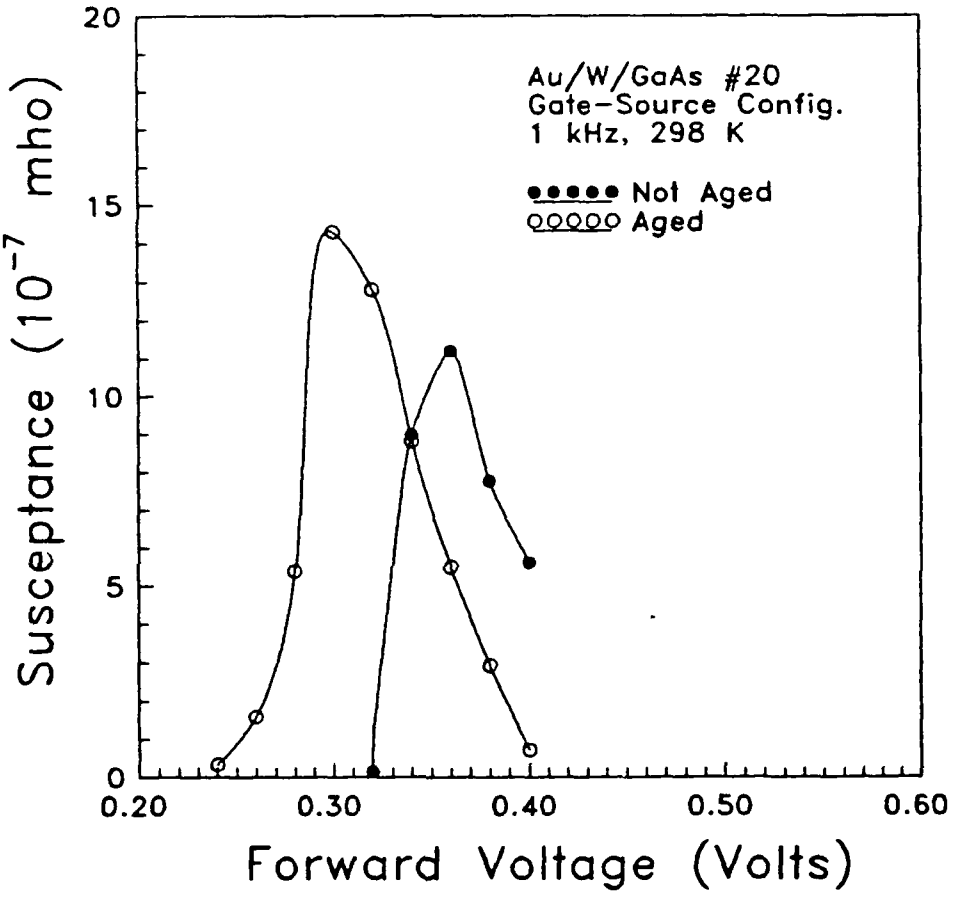

Fig. 10. Susceptance versus forward voltage for a typical Au/W/GaAs Schottky barrier in the not aged condition and after aging at -10 V for 12 hours. Measurement frequency was 1 kHz. Line is eye aid only.

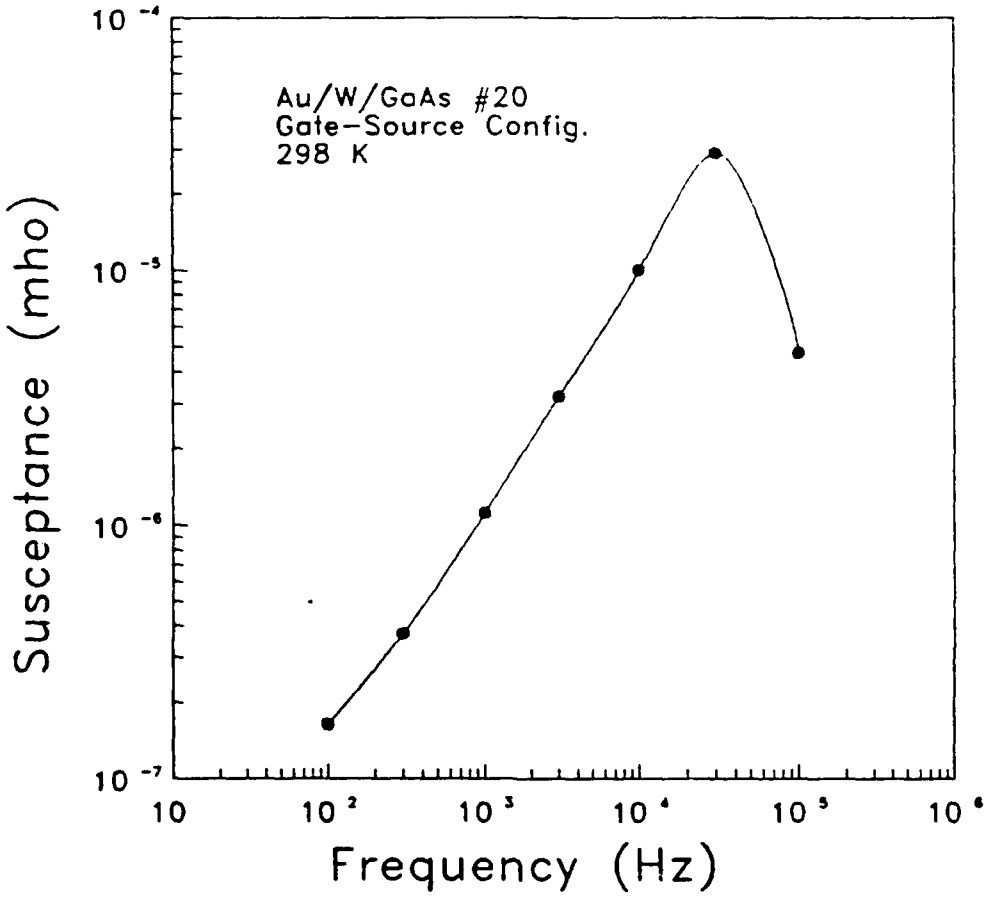

Fig. 11. Susceptance versus frequency for a typical not aged Au/W/GaAs sample. Aged data is similar within experimental error, and thus was not shown for clarity. Measurement voltage was 0.36 V. Line is eye aid only.

If this gate metalization (Au/W/GaAs) is taken to be typical for a non-reactive interface then the following should be noted. More native oxide is present, as has been evidenced in the increased oxide present in the Auger results,[8,17] in the larger ideality factor, and in the large discrepency between the measured Richardson constant and the theoretical one.[24] The aging process presumably involves the creation of interface-states, which then are able to change the barrier height. Note that, like the Au/Pt/Ti/GaAs samples, it is doubtful whether the interface-states control the barrier height in the non-aged condition, simply because there are not enough of them. However, it is clear that the interface-states being measured do at least influence, if not control the barrier height, once a certain concentration of them has been reached. Once again it is not possible to discern the role of fixed charge in this process.

As has been reported previously there is a mechanism by which most of the barrier height aging may be recovered. The samples were seen to recover most of their barrier height change if left to sit for for a few days or weeks at zero bias, or in a day or so if left under forward bias. It was initially thought that this forward bias technique would show the equivalence of the initial and the recovered stage in terms of the interface-state configuration, but at present the results seem to indicate at least one intermediate stage of recovery. Figure 12 attempts to show at least some of the complexity of the situation.

In this flow diagram a Au/W/GaAs diode (#38) is followed as it goes through the aging and recovery process. The sample initially has a barrier height of 0.729 eV, and an interface-state density in the low 10^{13} cm^{-2} eV^{-1} region. After aging for 12 hours with V_{gs} = -10 V the barrier height has dropped to 0.674 eV and the measured interface-state density has increased to

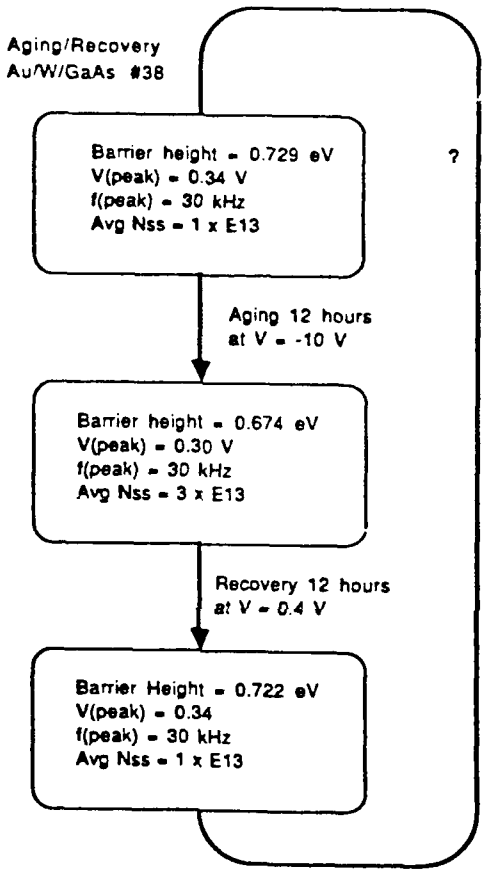

Fig. 12. Aging and recovery diagram for Au/W/GaAs sample #38. The question mark indicates the not understood process by which a forced recovery diode becomes identical to a not aged sample.

the mid 10^{13} cm^{-2} eV^{-1} range. This aging is then followed by recovery under forward bias (at V_{gs} = 0.5 V) for 12 hours. As has been reported previously, the recovery process is a logarithmic one, and as we see the barrier height has recovered close to, but not at its initial value.

It is a serious mistake to think that an age at this point will give results identical to that of a not aged (or at least naturally recovered) sample. Instead, an age here will result in yet another interface-state configuration (which seems to have a peak in its interface-state response at 10 rather than 30 kHz); one which seems to depend on how long the sample has been sitting before it is tested. For this reason the loop back to the initial state on Figure 12 is shown with a question mark on it to indicate a necessary, but not understood process, by which a forced recovery sample is converted back into its (nearly) not aged state.

Because of the poorly understood nature of this natural recovery process it was not possible at this point to perform several desirable experiments in a meaningful way. For example, is the aging process a linear one? Does the interface-state density track directly with the change in barrier height? Or, are there intermediate steps in the aging process, and we are only looking at the beginning and end? What is the voltage dependence of the aging process? Is an age at V_{gs} = -8 V the same as an age at V_{gs} = -10 V, only slower? In order to answer these questions it will be necessary to understand more fully the recovery process so that samples with the same initial energy state configuration can be employed.

V. CONCLUSIONS AND RECOMMENDATIONS

In this work the reasons why the barrier height of certain GaAs Schottky barriers decrease after being held for a long time at reverse bias have been examined. In particular we have looked for the influence of interface-states in this process. The method of Werner et al.,[15] which estimates interface-state concentrations from forward-bias conductance variations, was found not to be applicable because of the large conductance already present in these power MESFET samples. Instead, the experimental method used was forward bias capacitance, as developed by Wu and Yang.[14] Several key assumptions had to be made in order to use this method. The most important of these involved assuming donor type interface-states were involved which had a constant capture cross-section throughout the measurement cycle, including aging and recovery. Assumptions also had to be made concerning the nature of the interface involved with each of the type of samples.

With these assumptions in mind the average interface-state concentration of the Au/Pt/Ti/GaAs diodes was found to be in the low 10^{12} cm^{-2} eV^{-1} range. This value is consistent with the reactive nature of the interface, with relatively little oxide present there. This concentration of interface-states is probably not enough to account for the Fermi level pinning of these samples, and other reasons, perhaps fixed charge and/or deep traps, are responsible. As has been previously reported and repeated here these samples do not show significant aging characteristics.

In marked contrast are the Au/W/GaAs samples. Again with the same type of assumptions, the average interface-state density was found to be in the mid to upper 10^{12} cm^{-2} eV^{-1} range. Once again, particularily in the lower end

of this range, there are not enough interface-states to explain the Fermi-level pinning behavior. After aging these diodes in reverse bias the observed interface-state concentration has increased to the low to mid 10^{13} cm^{-2} eV^{-1} range, indicating interface-state generation has taken place. The pinning mechanism has apparently changed, and the generated interface-states now play at least some role in determining the barrier height.

There are several major unresolved issues which come out of this work. One of these is the role of deep levels in barrier height determination of these samples. Are deep levels responsible in any way for the Fermi-level pinning observed in these samples? Does the deep level configuration change in the aging process? A second unresolved issue involves the assumption of a constant capture cross section for these samples, including aged and recovered ones. Is this a reasonable assumption? A recent study involving hot-carrier damage in Si MOS structures makes one wonder.[23] The study funded by AFOSR/UES for 1989 using DLTS techniques will be looking for evidence of deep levels and/or interface-states in these samples. It is particularily hoped that interface-states will be observed, both as an independent confirmation of what has been observed here and perhaps as a way of measuring the capture cross section in the manner recently suggested by Vuillaume et al.[23]

Another major unresolved issue is the role of fixed charge in determining the barrier height of these samples. A recent study by Sobolewski and Helms[28] has indicated that fixed charge and band lineup determine the barrier height of their metal - silicon nitride - silicon Schottky barriers. It is not possible to examine the role of fixed charge in a similar manner with the samples used here because of the requirement of a variety of nitride (oxide) thicknesses. One possible direction might be to fabricate a

series of diodes in a manner similar to Sobolewski and Helms, and then evaluate the role of fixed charge in these structures. This would also help in one of the major assumptions for the evaluation of the *interface-state density*, where the thickness of the interfacial region would be accurately known for these samples, rather than having to be estimated.

Other unresolved issues involve the nature of the aging and recovery process observed. It was not possible in the limited time duration of this project to examine the variation between the natural recovery process and the forced one. Thus, it was also not possible to track the kinetics of the aging process due to the lack of a reproducible recovery cycle, because every age after the first one started from a different interface-state configuration.

The measurements needed to understand the aging and recovery cycles could be made in a much more expedious manner if the apparatus were built in an automated fashion. The increased speed of an automated bridge would also help allieviate any recovery processes that are taking place during the forward bias measurement. In addition, the next version of the apparatus should contain some way of varying the sample temperature, so that an estimation of the interface-state density as a function of energy across the bandgap could be made. This sort of information would help in attempting to make an identification of the physical species involved in these interface-states.

VI. ACKNOWLEDGEMENTS

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APPENDIX:
DERIVATION OF THE FORWARD-BIAS CAPACITANCE EXPRESSION FOR A SCHOTTKY BARRIER

Preface:

It is intended that this Appendix will serve two purposes. First, it will act in a general way to indicate why forward bias capacitance should be present in the Schottky diode structures examined in this study. Secondly, it will attempt to fill in several missing points in the origional derivation by Wu and Yang.[14] It is best considered as a supplement to, rather than a replacement for, the derivation given by Wu and Yang.

Introduction:

First it is assumed that in forward bias the current density of a Schottky barrier is given by Thermionic emission as:

$$J_n = \left(A^* T^2 \exp\left(\frac{-q\phi_B}{kT} \right) \right) \left(\exp \frac{qV_F}{kT} - 1 \right). \qquad \text{A-1}$$

where J_n is the current density, A^* is the effective Richardson constant, T is the temperature, ϕ_B is the barrier height, k is Boltzman's constant, q is the electron charge, and V_F is the forward voltage. If now $V_F >> kT/q$, S is the area, and n is the ideality factor, then the current is given by:

$$I_n = \left(S A^* T^2 \exp\left(\frac{-q\phi_B}{kT} \right) \right) \left(\exp\left(\frac{q V_F}{nkT} \right) \right). \qquad \text{A-2}$$

The non-ideality in a Schottky may be taken as a combination of several

different effects. There is a bias dependence of the barrier height, both through image force lowering (which is usually quite small and therefore neglected) and through the effect of an insulating interfacial layer. A second major effect is due to electron tunneling through the barrier, resulting in a contribution from Field (F) or Thermionic-Field (TF) emission. Neither of these alternate current flow mechanisms has been seen in the forward bias characteristics of the samples tested. A third possible reason for non-ideality is carrier recombination in the depletion region, which occurs if the carrier concentration is less than about 10^{15} cm^{-3} (which is two orders of magnitude less than the carrier concentrations of the MESFET channels examined here). A final contribution to non-ideality is possible from a combination of substrate and contact resistance. For this derivation the non-ideality will be attributed to the combination of an insulating interfacial layer along with any substrate resistance.

The current may then be written as:

$$I_n = S\, A^*\, T^2 \exp\left(\frac{-q}{kT} \left(\phi_B + \phi_S - V + R_S I \right) \right) \qquad \text{A-3}$$

where ϕ_S is the voltage drop at the interface and $R_S I$ is the voltage drop across the substrate and contact region.

If now a small ac signal is superimposed on the dc signal the voltage and current may be written as:

$$V = V + \Delta V \qquad \text{A-4}$$

and

$$I = I + \Delta I \qquad \text{A-5}$$

where ΔI will be desiginated i. The current may now be written as:

$$I + i = S A^{*} T^{2} \exp\left(\frac{-q}{kT} \left(\phi_B + \phi_S + \Delta\phi_S - V - \Delta V + R_S I + R_S i \right) \right) \quad \text{A-6}$$

Remembering equation A-3, and also since exp(a + b) = (exp a)(exp b), then

$$I + i = I \exp\left(\frac{q}{kT} \left(\Delta V - \Delta\phi_S - R_S i \right) \right) \quad \text{A-7}$$

If i is now solved for, then

$$i = I \exp\left(\frac{q}{kT} \left(\Delta V - \Delta\phi_S - R_S i \right) \right) - I \quad \text{A-8}$$

A McLarin series expansion is now used on the exponential term, and after rearranging the small signal ac current may be written as

$$i = I \frac{q}{kT} \frac{\left(\Delta V - \Delta\phi_S \right)}{\left(1 + I \frac{q}{kT} R_S \right)} \quad \text{A-9}$$

Remembering the definition for admittance,

$$Y = \frac{\Delta I}{\Delta V} = \frac{i}{\Delta V} \quad \text{A-10}$$

then the admittance for this situation may be written as:

$$Y = \frac{Iq}{kT} \frac{\left(1 - \frac{\Delta\phi_s}{\Delta V}\right)}{\left(1 + \frac{Iq}{kT} R_S\right)} \quad \text{A-11}$$

Complex Nature of the Barrier Height:

The admittance can be written in general as the sum of a real plus an imaginary part, called the conductance and the susceptance, respectively. If the susceptance is strictly due to capacitance than the admittance can be written as:

$$Y = G + jB = G + j\omega C \quad \text{A-12}$$

The barrier height will also be written as a complex quantity, with the following definitions: $\Delta\phi_{SR}$ is the real part, and $\Delta\phi_{SI}$ is the imaginary part of of $\Delta\phi_S$. The change in barrier height may then be written as:

$$\Delta\phi_S = \Delta\phi_{SR} + j\,\Delta\phi_{SI} \quad \text{A-13}$$

This definition is substituted back into the admittance expression and G and B are solved for with the following results:

$$G = I\frac{q}{kT} \frac{\left(1 - \frac{\Delta\phi_{SR}}{\Delta V}\right)}{\left(1 + I\frac{q}{kT} R_S\right)} \quad \text{A-14}$$

$$B = \omega C = I \frac{q}{kT} \frac{\left(\frac{-\Delta\phi_{SI}}{\Delta V} \right)}{\left(1 + I \frac{q}{kT} R_S \right)} \qquad \text{A-15}$$

In the next section of the discussion the physical significance of the barrier height change at the interface will be disussed, particularily the imaginary component there. This will be dealt with in terms of a charge capture process at the interface-states, which gives an out of phase signal. This out of phase signal in turn gives rise to the capacitance in forward bias. Starting with Gauss' law,

$$\Delta\phi_S = -\left(\frac{\Delta Q}{C_i} \right) = -\left(\frac{\Delta Q_{SS} + \Delta Q_{SC}}{C_i} \right) \qquad \text{A-16}$$

where ΔQ_{SS} is the interface charge, ΔQ_{SC} is the depletion layer charge, and C_i is the interface specific capacitance. If it is assumed that the depletion layer charge is mostly in phase with the applied voltage and additionally of magnitude less than the interface charge, then the imaginary component of the barrier height change at the interface may be written as:

$$\Delta\phi_{SI} = -\left(\frac{\Delta Q_{SS}}{C_i} \right) \qquad \text{A-17}$$

In order to solve for this change in barrier height it will be necessary to know the interface charge, which in turn relies on knowledge of the density of interface-states and their occupation, since:

$$\Delta Q_{SS} = -\, q \int N_{SS}(E)\, \delta f(E)\, dE \qquad \text{A-18}$$

where $N_{SS}(E)$ is the density of interface states at an energy E and $\delta f(E)$ is the increment of occupation probability of these states due to the ac current flow.

Evaluation of Interface-State Occupation:

The evaluation of this occupation has been done using Schockley-Read statistics by Wu and Yang[14] and only the result is repeated here:

$$\delta f = \frac{c_n (1 - f)\,\delta n_S}{c_n n_{SO} + {}^{1}/_{\tau_M} + j\omega} \qquad \text{A-19}$$

where c_n is capture coefficient for electrons, f is the steady state occupation of these states, δn_S is the variation of n_S, n_{SO} is the free electron density at the semiconductor surface under forward bias, τ_M is the metal-interface relaxation time, and ω is the angular frequency. Now let

$$N_S\left(E_f^S\right) = \int_{E_f^M}^{E_f^S} N_{SS}(E)\,dE \qquad \text{A-20}$$

then upon substitution of A-18, A-19, and A-20 back into A-17 the following expression is obtained:

$$\Delta\phi_S = \frac{q\,N_S\left(E_f^S\right)}{C_i} \frac{c_n (1 - f)\,\delta n_S}{c_n n_{SO} + {}^{1}/_{\tau_M} + j\omega} . \qquad \text{A-21}$$

Susceptance:

This expression can then be simplified by multiplying by $c_n n_{S0} + 1/\tau_M - j\omega$ / $c_n n_{S0} + 1/\tau_M - j\omega$. After gathering terms the real and imaginary parts of the expression can be separated, with the imaginary portion, corresponding to the susceptance, shown below:

$$B = \frac{I q}{kT} \frac{1}{\left(1 + \frac{I q R_S}{kT}\right)} \left(\frac{-1}{\Delta V} \frac{q N_S(E_f^S)}{C_i} \frac{c_n (1 - f) \delta n_S(-\omega)}{\left(c_n n_{S0} + 1/\tau_M\right)^2 + \omega^2} \right). \qquad \text{A-22}$$

Because of the difficulty in estimating values for the capture coefficients, these are replaced with capture cross sections by noting that

$$c_n = \sigma_n \bar{v} \qquad \text{A-23}$$

where σ_n is the capture cross section and v is the average velocity. Also, since

$$J = \frac{q \bar{v} n_{S0}}{4} \qquad \text{A-24}$$

and

$$j = \frac{q \bar{v} \delta n_{S0}}{4} \qquad \text{A-25}$$

then

$$c_n n_{S0} = \sigma_n \bar{v} n_{S0} = 4 \sigma_n J / q \qquad \text{A-26}$$

and

$$c_n \delta n_{S0} = \sigma_n \bar{v} \delta n_{S0} = 4 \sigma_n j/q. \qquad \text{A-27}$$

With these expressions substituted back into equation A-22 the final expression for the susceptance is obtained:

$$B = \frac{q^2 I}{kT\left(1 + I\frac{q R_S}{kT}\right)} \frac{N_S\left(E_f^S\right)}{C_i \Delta V} \frac{\omega(1-f)4\sigma_n j/q}{\left(4\sigma_n J/q + 1/\tau_M\right)^2 + \omega^2} \qquad \text{A-28}$$

The experimental data is then curve fitted to this expression as explained in the main portion of the text.